

RC5034

High Accuracy Synchronous DC-DC Converter

Features

- Pentium™ VREF; 2% accuracy
- >85% Efficiency
- 350uA quiescent current in shutdown
- Fast transient response
- Soft control power-up
- Over-Voltage Protection
- Factory trimmed low TC reference voltage
- Adjustable oscillator frequency
- Drives N-Channel MOSFETs; to 1 MHz
- 16 pin SOIC package

Applications

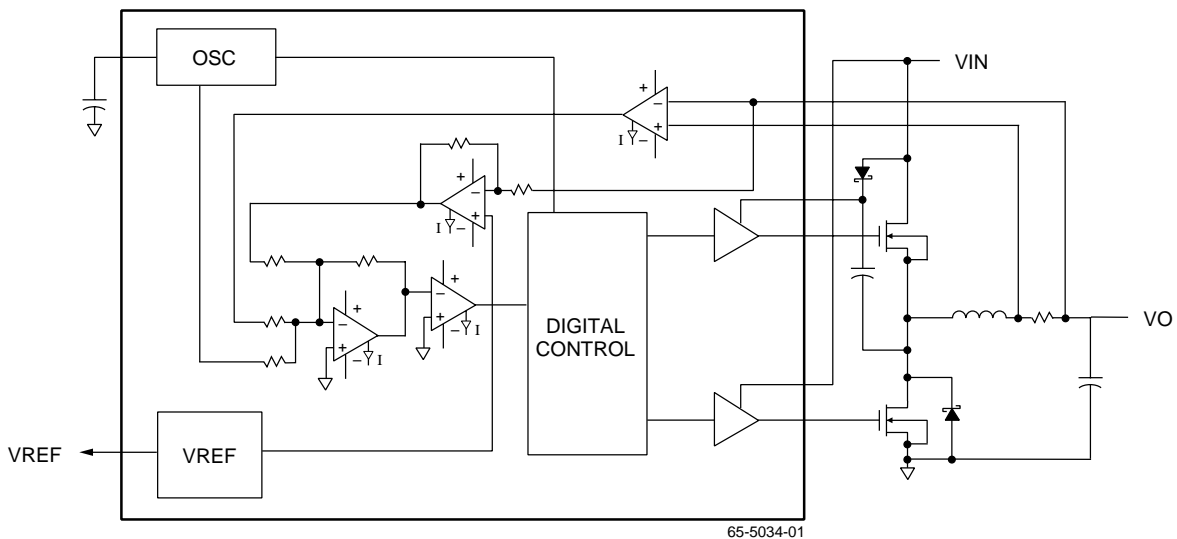
- 3.3V power supply for Pentium™ based CPUs requiring 2% VRE specification motherboards

Description

The RC5034 is a synchronous mode DC-DC controller IC dedicated to providing a 5V to 3.52V conversion for Pentium™ CPUs that require the 2% VRE voltage specification. It can be configured in both the synchronous and non-synchronous modes and with the proper applications circuitry can be used to deliver load current greater than 10 Amps. The RC5034 is designed to operate in a standard PWM control mode under heavy load conditions and as a PFM controller in light load conditions. Its highly accurate

low TC reference eliminates the need for precision external components in order to achieve tight tolerance voltage regulation. An integrated Over-Voltage protection function constantly monitors the output voltage and shuts down the power to the CPU in the event of a out-of-tolerance voltage situation, thereby protecting the CPU. The programmable oscillator can operate from 200KHz to greater than 1MHz to provide for flexibility in choosing external components such as inductors, capacitors, and Power MOSFETs.

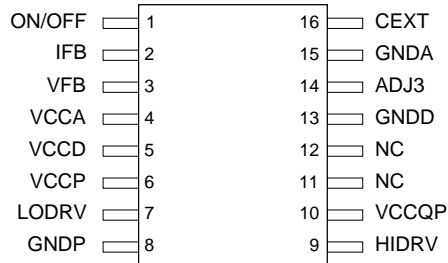
Block Diagram



Rev. 0.9.6

PRELIMINARY INFORMATION describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Raytheon for current information.

Pin Assignments



65-5034-02

Pin Definitions

Pin Name	Pin Number	Pin Function Description
On/Off	1	A low level on this pin will power down; tie to VCCD if not used.
IFB	2	Current Feedback Input.
VFB	3	Voltage Feedback Input.
VCCA	4	Analog VCC.
VCCD	5	Digital VCC.
VCCP	6	VCC for synchronous FET output drivers.
LODRV	7	Synchronous FET driver output.
GNDP	8	Power ground for high current drivers.
HIDRV	9	High side FET driver output.
VCCQP	10	VCC for High side FET output driver
NC	11, 12	No Connections leave open
GNDD	13	Digital ground.
ADJ3	14	VREF
GNDA	15	Analog ground.
CEXT	16	External capacitor for setting oscillator frequency.

Absolute Maximum Ratings

(beyond which the device may be damaged)¹

Parameter	Conditions	Min	Typ	Max	Units
VCCP	Low Driver Supply			13	V
VCCQP	High Driver Supply			13	V
T _J	Junction Temperature			175	°C
T _A	Ambient Operating Temperature	0		70	°C
T _S	Storage Temperature	-65		150	°C
T _L	Lead Soldering Temperature	(10 seconds)		300	°C

Note:

1. Functional operation under any of these conditions is NOT implied.

Preliminary Information

Operating Conditions

Parameter		Conditions	Min	Typ	Max	Units
VCC	Supply Voltage		4.5	5	7	V
VCCP	Low Driver Supply		4.5	5	7	V
VCCQP	High Driver Supply		9		13	V
VIH	Input Voltage, Logic HIGH		2			V
VIL	Input Voltage, Logic LOW				0.8	V

DC Electrical Characteristics

(VCC = 5V, fosc = 650 KHz, and TA = +25°C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
VO	Output Voltage	TA = 0–70°C	3.45	3.52	3.6	V
IO	Output Current	See Figure 1 for application		5		A
Vref Acc	Reference Acc			.15	1	%
VTC	Output Voltage TC			-40		ppm
LDR	Load Regulation	0.5 to 7A		0.25		%Vo
LIR	Line Regulation	VCC = ±5%		0.1		%Vo
VR	Output Voltage Ripple			15		mV
Cum Acc	Cumulative Accuracy ²	TA = 0–70°C		1	2.1	%
Eff	Efficiency	Synchronous mode > 2A	85	88		%
Iodr	Output Driver I	Open Loop	0.5	0.7		A
Pd	Power Dissipation			0.1	0.2	W

Notes:

- Functional operation under any of these conditions is not implied. Performance is guaranteed only if Operating Conditions are not exceeded.
- Output Voltage accuracy, Tempco, load regulation, ripple, and transient performance determine the Cumulative Accuracy.

AC Electrical Characteristics¹

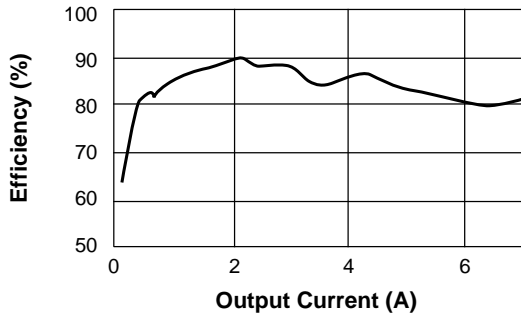
(VCC = 5V, fosc = 650 KHz, and TA = +25°C unless otherwise noted)

Parameter		Conditions	Min	Typ	Max	Units
Tr	Response Time	II=0.5A to 5.5A		10		μs
Fosc	Oscillator Range		0.2		1.2	MHz
Osc Acc	Fosc Accuracy			10		%
Dtc	Max Duty Cycle	PWM mode	90	95		%
Dtcm	Min Duty Cycle	PFM mode			100	ns
Imax	Imax Threshold			30		mV
Iscp	Short Circuit Prot			80		mV
Ovp	Over Voltage Prot			20		%Vo
Trimax	Response to Imax			15	30	ns
Tssp	Soft start response			10		μs

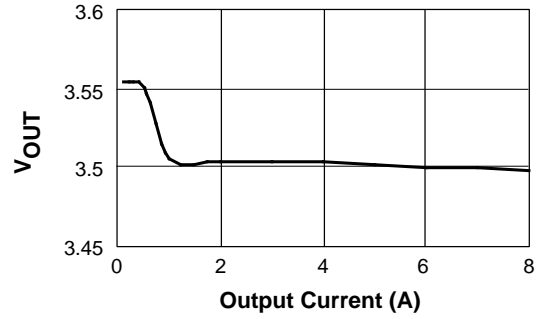
Typical Operating Characteristics¹

Preliminary Information

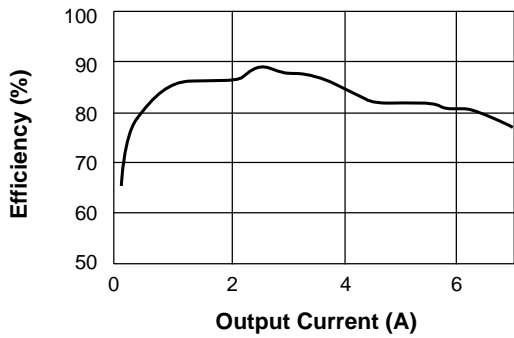
Efficiency vs Output Current ($F_{OSC} = 400 \text{ KHz}$)



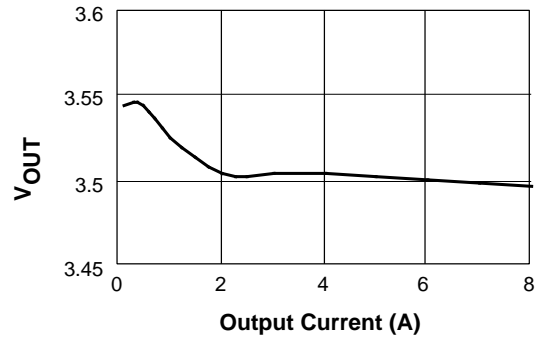
Load Regulation ($F_{OSC} = 300 \text{ KHz}$)



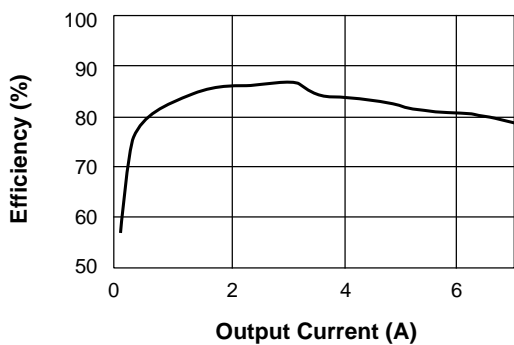
Efficiency vs Output Current ($F_{OSC} = 650 \text{ KHz}$)



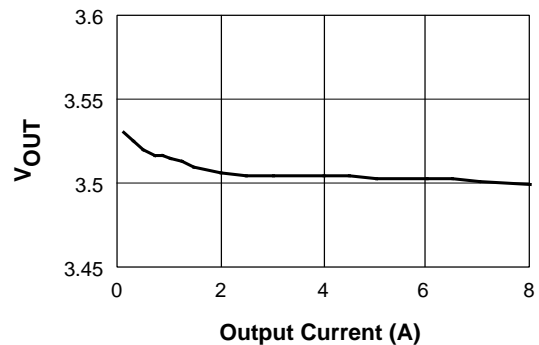
Load Regulation ($F_{OSC} = 650 \text{ KHz}$)



Efficiency vs Output Current ($F_{OSC} = 1 \text{ MHz}$)



Load Regulation ($F_{OSC} = 1 \text{ MHz}$)



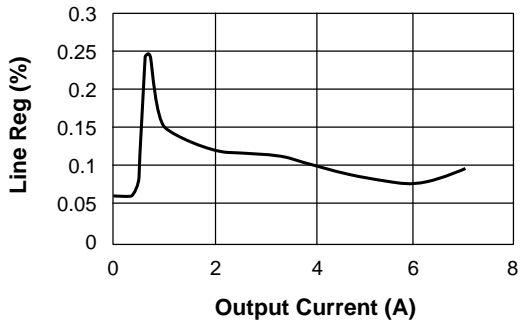
65-5034-03

Note:

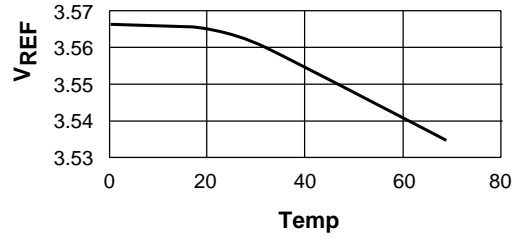
1. Data taken with circuit of Figure 1.

Typical Operating Characteristics (continued)

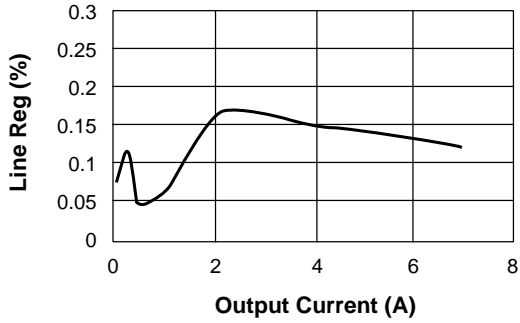
Line Regulation vs. Output Load
(F_{OSC} = 400 KHz)



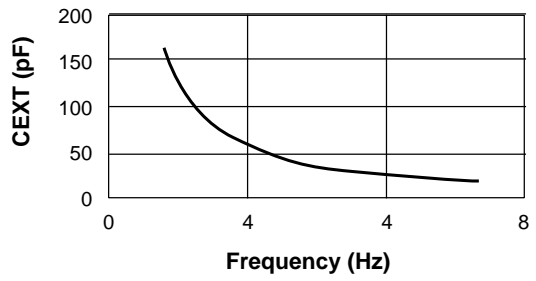
Reference Tempco



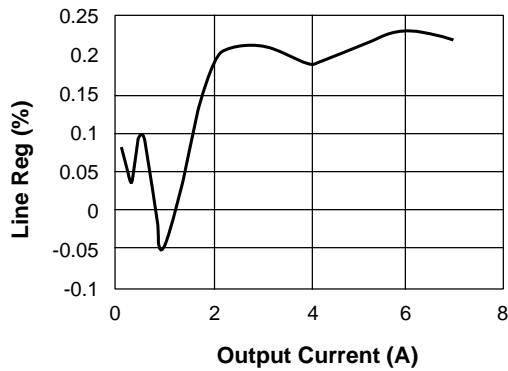
Line Regulation vs. Output Load
(F_{OSC} = 650 KHz)



CEXT vs. Oscillator Frequency



Line Regulation vs. Output Load
(F_{OSC} = 1 MHz)

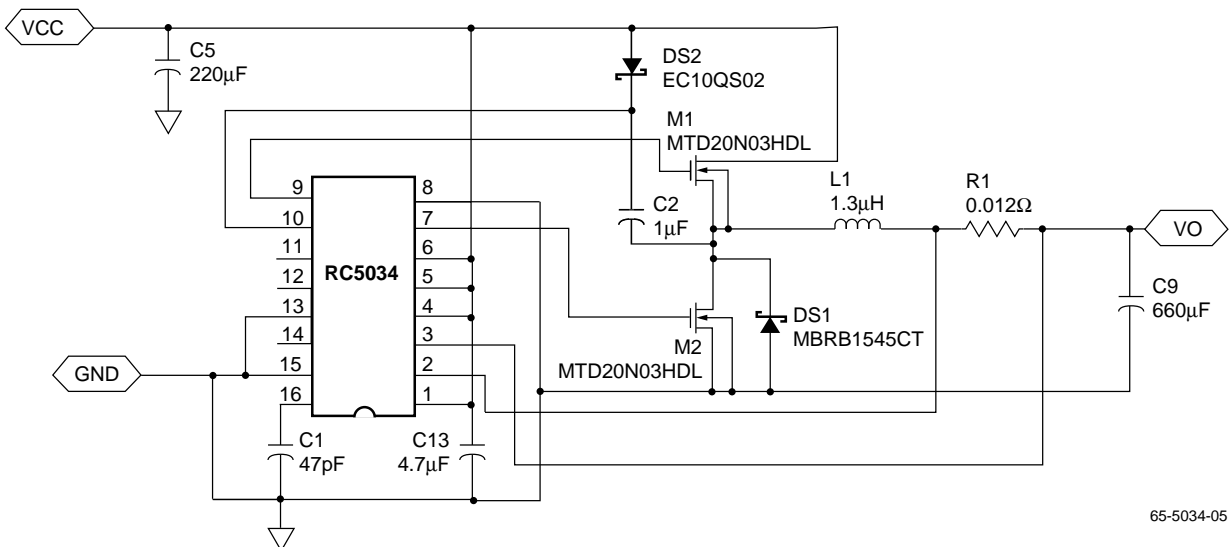
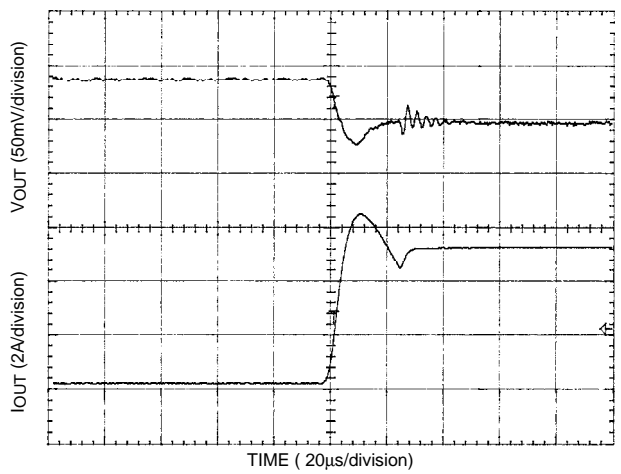
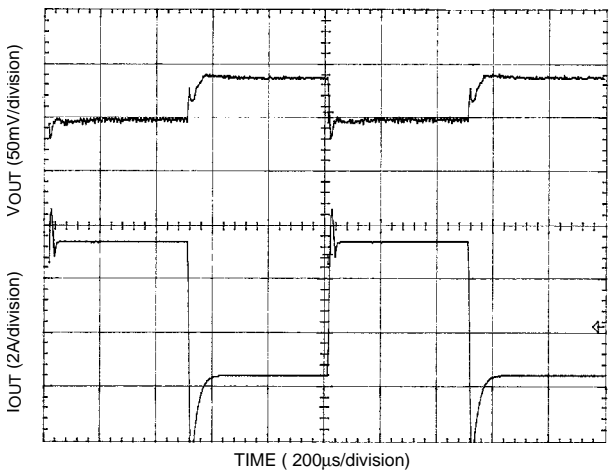
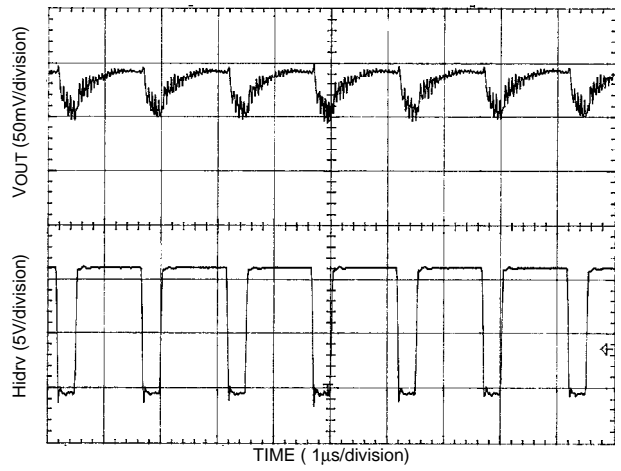
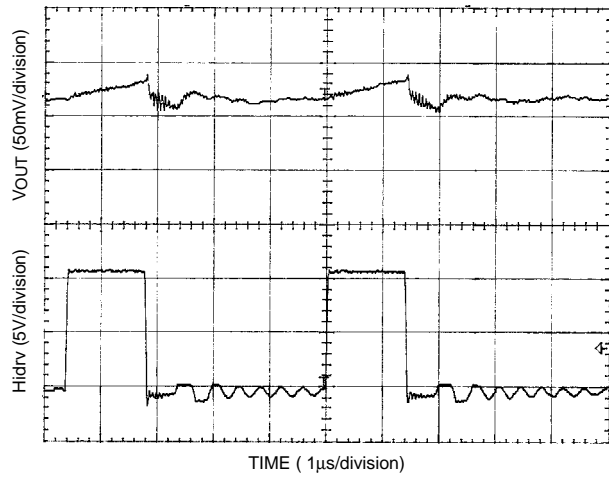


65-5034-04

Preliminary Information

Typical Operating Characteristics (continued)

Preliminary Information



65-5034-05

Figure 1. Synchronous 7A Schematic

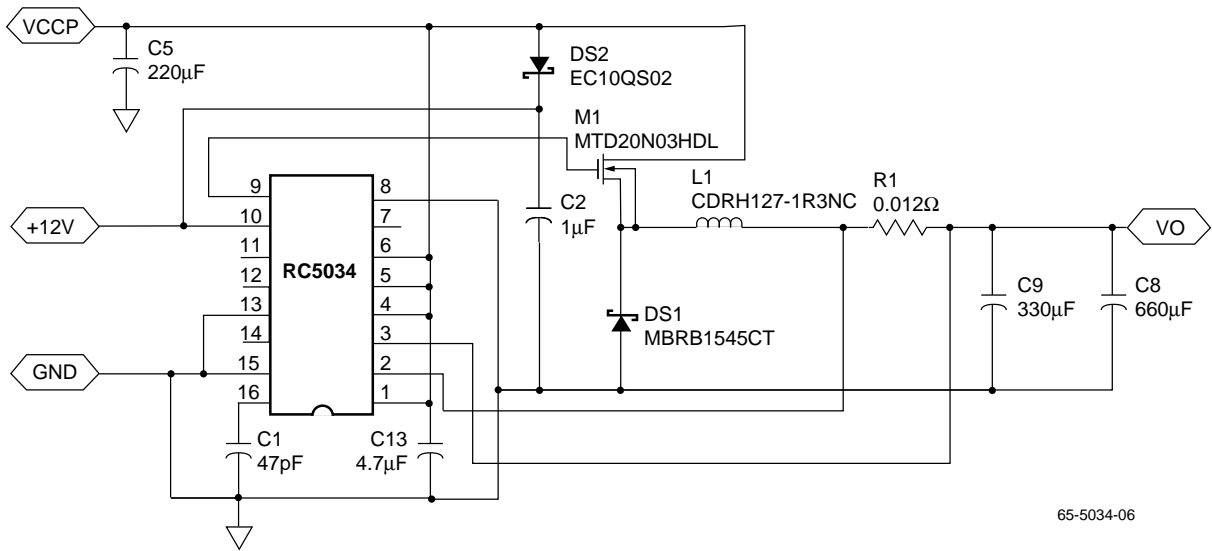


Figure 2. Non-Synchronous 7A Circuit

RC5034 Standard Application Circuit Bill of Materials			
Ref Designator	Quantity	Part No.	Manufacturer
L1	1	1.3 μ H CDRH127-1R3NC	Sumida
M1,M2	2	MTD20N03HDL	Motorola
DS1	1	MBRB1545CT	Motorola
DS2	1	EC10QS02L	Nihon
R1	1	.012 Ω LRC-2512	IRC
C5	1	220 μ F OS-CON 10SA220M	Sanyo
C9	2	330 μ F OS-CON 10SA330M	Sanyo
C2	1	1uF	Monolithic ceramic Cap
C1	1	47pF	SMD Cap
C4	2	0.1uF	SMD Cap
C13	1	4.7uF	SMD Cap

Table 1. Components for RC5034

RC5034 Alternate Suppliers of Components			
Ref Designator	Quantity	Alternate Part No.	Alternate Manufacturer
L1	1	1.3 μ H PE-53680	Pulse Engineering
M1,M2	2	2SK1388	Fuji
		IRLZ44N	International Rectifier
		Si4410DY	Temic (Siliconix)
DS1	1	C10T02QL	Nihon
		SR1620C	Rectron
DS2	1	MBRS140T3	Motorola
R1	1	.012 Ω WSL-2512	DALE

Table 2. Alternate Components Selection

Preliminary Information

Main Control Loop

The main control loop of the regulator (see Block Diagram) contains two main blocks, the analog control block and the digital control block. The analog control block consists of signal conditioning amplifiers that feed into a set of fast comparators which provide the inputs to the digital control block. The signal conditioning block takes inputs from the IFB(current feedback) and VFB(voltage feedback) pins and then sets up two controlling signal paths. The voltage control path gains up the VFB signal and presents that signal to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents that signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator and the output is then presented to a comparator. This comparator provides the main PWM control signal to the digital control block.

There are three other comparators in the analog control block. The first two control the thresholds of where the RC5034 goes into its pulse skipping mode during light loads and the second controls the point at which the max current comparator disables the output drive signal to the upper power MOSFET. The third comparator determines when the synchronous mode bottom side power MOSFET will be enabled and disabled.

The digital controller section is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the HIDRV and LODRV output pins that will in turn control the external power MOSFETs. This digital section was designed in high speed schottky transistor logic which allows the RC5034 to clock up to speeds greater than 1MHz. This section is responsible for providing the break-before-make timing that ensures that both external FETs will not be on at the same time.

High Current Output Drivers

The RC5034 contains two identical high current output drivers. These drivers contain high speed bipolar transistors configured in a push-pull configuration. Each output driver is capable of pumping out 1A of current in less than 100ns. Each driver's power and ground are separated from the overall chip power and ground for added switching noise immunity. The HIDRV driver has a power supply, VCCQP, which can be either derived from an external voltage source or can be boot-strapped from a flying-capacitor as is shown in Figure 1. In the boot-strapped mode, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when M1 is turned on. This provides a VCCQP voltage equal to $2 \cdot VCC - V_{ds}(DS2)$; or about 9.5V with $VCC=5V$. This voltage is sufficient to provide the 9V gate drive to the external MOSFET that will be needed for achieving a low $R_{ds(on)}$. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can just be tied to VCC.

Internal Reference

The reference in the RC5034 is a precision band-gap type reference. Its temperature coefficient is trimmed to provide a near zero TC. For a guaranteed stable operation under all loading conditions, a 0.1 μ F capacitor is recommended on the VREF output pin.

Over -Voltage Protection

The RC5034 provides a constant monitor of the output voltage for over-voltage protection. Should the voltage at the VFB pin exceed 20% of the selected program voltage, then an overvoltage condition will be assumed to exist and the RC5034 will shut down the output drive signals to the power FETs.

Oscillator

The RC5034 oscillator is designed as a fixed current capacitor charging oscillator. An external capacitor allows for maximum flexibility in choosing the associated external components for the RC5034. The oscillator frequency can be set from less than 200KHz to over 1MHz depending on the application requirements.

Design Procedure and Applications Information

Simple Step-Down Converter

Figure 4 shows a step-down DC-to-DC Converter with no feedback controller. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5034 in Figure 1. In Figure 4, the basic operation begins by closing the switch, S1. When S1 is closed the input voltage V_B is impressed across the inductor L1. The current flowing in the inductor is given by the following equation: $I_L = (V_B - V_o)T_{on}/L$; where T_{on} is the time duration for S1 to be closed. When S1 is open, the diode will conduct the inductor current and the output current will be delivered to the load according to the equation: $I_L = V_o(T - T_{on})/L$; where $T - T_{on}$ is the time duration for S1 to be off. By solving these two equations we can arrive at the basic relationship for the output voltage of a step-down converter: $V_o = V_B(T_{on}/T)$.

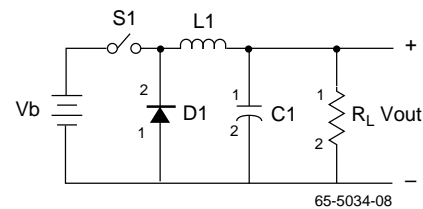


Figure 4. Simple Buck DC-DC Converter

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-to-DC converter application. The critical parameters are inductance (L), max DC current (Imax), and the coil resistance (RI). The inductor core material is a critical factor in determining the amount of current that the inductor will be able to handle. As with all engineering designs there are trade-offs for various types of inductor core materials. In general, Ferrites are popular because of their low cost, low EMI, and high frequency (>500kHz) characteristics. Molypermalloy powder (MPP) materials have good saturation characteristics and low EMI with low hysteresis losses; however they tend to be expensive and are more efficiently utilized at frequencies below 400kHz. DC winding resistance is another critical parameter. In general, the DC resistance should be kept as low as possible. The power loss in the DC resistance will degrade the efficiency of the converter by the relationship: Power Loss = (Io)2*RI.

The value of the inductor is a function of the switching frequency (Ton) and the maximum inductor current. The max inductor current can be calculated from the relationship:

$$I_{MAX} = \frac{2I_L}{F_o T_{ON} \left(\frac{V_{IN} - V_{OUT}}{V_{OUT} - V_D} \right) + 1}$$

Where: Fo is the desired clock frequency
 Ton is the max on time of the M1 FET
 Vd is the forward voltage of the schottky diode D1

Then the inductor value can be calculated with the relationship:

$$L = \frac{V_{IN} - V_{DSON}}{I_{MAX}} (T_{ON})$$

Where: Vdson is the voltage across the drain-source of the M1 FET when switched on.
 (this can be calculated by RDSon * Imax)

Current-Sense Resistor

The current sense resistor will carry all of the peak current of the inductor. This current will be more than the designed for load current. The RC5034 will begin to limit the output current to the load by turning off the top-side FET driver when the voltage across the current-sense resistor exceeds 100mV. When this happens the output voltage will temporarily go out of regulation. As the voltage across the resistor becomes larger, the top-side FET will turn off more and more until the current limit value is reached and then the RC5034 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. Thus the resistor should be set by the relationship:

$$R = 100 \text{ mV} / I_{peak}$$

Where: Ipeak = Imax * 1.33

Since the value of the sense resistor is generally in the milliohm region, care should be taken in the layout of the PCB. Trace resistance can contribute significant errors. The traces to the IFB and VFB pins of the RC5034 should be Kelvin connected to the pads of the current-sense resistor as shown in the sample layout Figure 5. To minimize the influence of noise the two traces should be run next to each other and the pins should be bypassed with a .1uF to GND as close to the device pins as possible.

Filter Capacitors

Good ripple performance and transient response are functions of the filter capacitors. Since the 5V input for a PC motherboard can be located several inches away from the DC-to-DC converter, input capacitance can play an important role in the load transient response of the RC5034. In general, the higher the input capacitance, the more charge storage is available for improving the current transfer through the top-side FET. A good rule of thumb is that for each watt of output power that you wish to deliver, there should be around 10uF of input capacitance. Low “ESR” capacitors are best suited for this application and can have an influence on the converter’s efficiency. The input capacitor should be placed as close to the drain of the top-side FET as possible to reduce the effect of ringing that can be caused by large trace lengths.

The ESR rating of a capacitor is a difficult number to pin down. ESR or Equivalent Series Resistance, is defined at the resonant impedance of that capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for it to have an associated resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained with the following equation: ESR = Pd/2pfC. Where Pd is the capacitor’s dissipation factor and f is the frequency of measure and C is the capacitance in farads.

With this in mind, calculating the output capacitance correctly is crucial to the performance of the DC-to-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and the transient load response. The calculation uses the following equation:

$$C (\mu F) = \frac{T_{ON} \left(\frac{(V_{IN} - V_{OUT}) I_{MAX}}{V_{OUT}} + I_L \right)}{V_r}$$

Where: Vr is the desired output ripple voltage

Schottky Diode Selection

The application circuit diagram shows two schottky diodes, DS1 and DS2. DS1 is used in parallel of M2 in order to prevent the lossy body diode in the FET from turning on. DS2 serves a dual purpose. As it is configured, it allows the VCCQP supply pin of the RC5034 to be bootstrapped up to 9V by using the bootstrap capacitor C2. When the lower FET

M2 is turned on, one side of the capacitor C2 is connected to GND while the other side of the cap is being charged up through D2 to a voltage that is $V_{in} - V_d$. When the lower FET turns off and the upper one turns on, the voltage that is supplied to the VCCQP pin is $2V_{in} - V_d$. The voltage then that is applied to the gate of the FET is $V_{CCQP} - V_{sat}$, typically around 9V. It is important in the selection of DS1 and DS2 that they have a low forward voltage drop as this directly affects the regulator efficiency. The other job that DS2 performs is that of bootstrapping VCCQP during startup. It is possible to cause the output stage to latchup if the VCCQP supply is brought up before the other VCC supplies of the RC5034. It is therefore advisable that DS2 be connected even in applications that do not utilize the bootstrapping technique for VCCQP. An alternate application could tie the VCCQP supply pin to the +12V power supply in the PC, thus eliminating the need for C2 and forcing the R_{dson} of M1 even lower by increasing its V_{gs} .

MOSFET Switches

The MOSFET switches in the RC5034 applications circuit are N-channel “logic-level” FETs. This means that they will be fully on with a V_{gs} of 4V. Many manufacturers make logic-level FETs and the trick is to choose the one with the lowest R_{dson} at the given I_{max} current level. The value of R_{dson} directly enters into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5034. At higher clocking rates the amount of charge needed to be

delivered to the FET is going to lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater current capability; however, the lower FET doesn’t necessarily have to be doubled since it is on only a fraction of the time that the upper FET is on.

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimum in the overall performance of the DC-to-DC converter. In general, it is always a good practice to have a tight layout that attempts to minimize short low inductance wiring to the RC5034.

The use of multilayer PCB is recommended. In particular, it is recommended to have a continuous ground plane beneath the circuit, 2oz copper would be preferred in high current applications. As was stated previously, the current-sense resistor, R1, should be located as close to the RC5034 as possible and the IFB and VFB traces should be Kelvin connected to the pads of R1. To minimize switching losses and noise, place M1, M2, L and DS2 as close together as possible. Also try to keep the HIDRV and LODRV gate drive signal traces as short as possible. It is recommended that the noisy switching part of the circuit be kept away from the low current pins on the chip such as IFB, VFB, ADJ3, ADJ1, and CEXT. Keep the 0.1uF bypass capacitors as close to the chip pins as possible. All of the ground pins should be connected to the ground plane directly under the chip. A sample layout is provided in Figure 5.

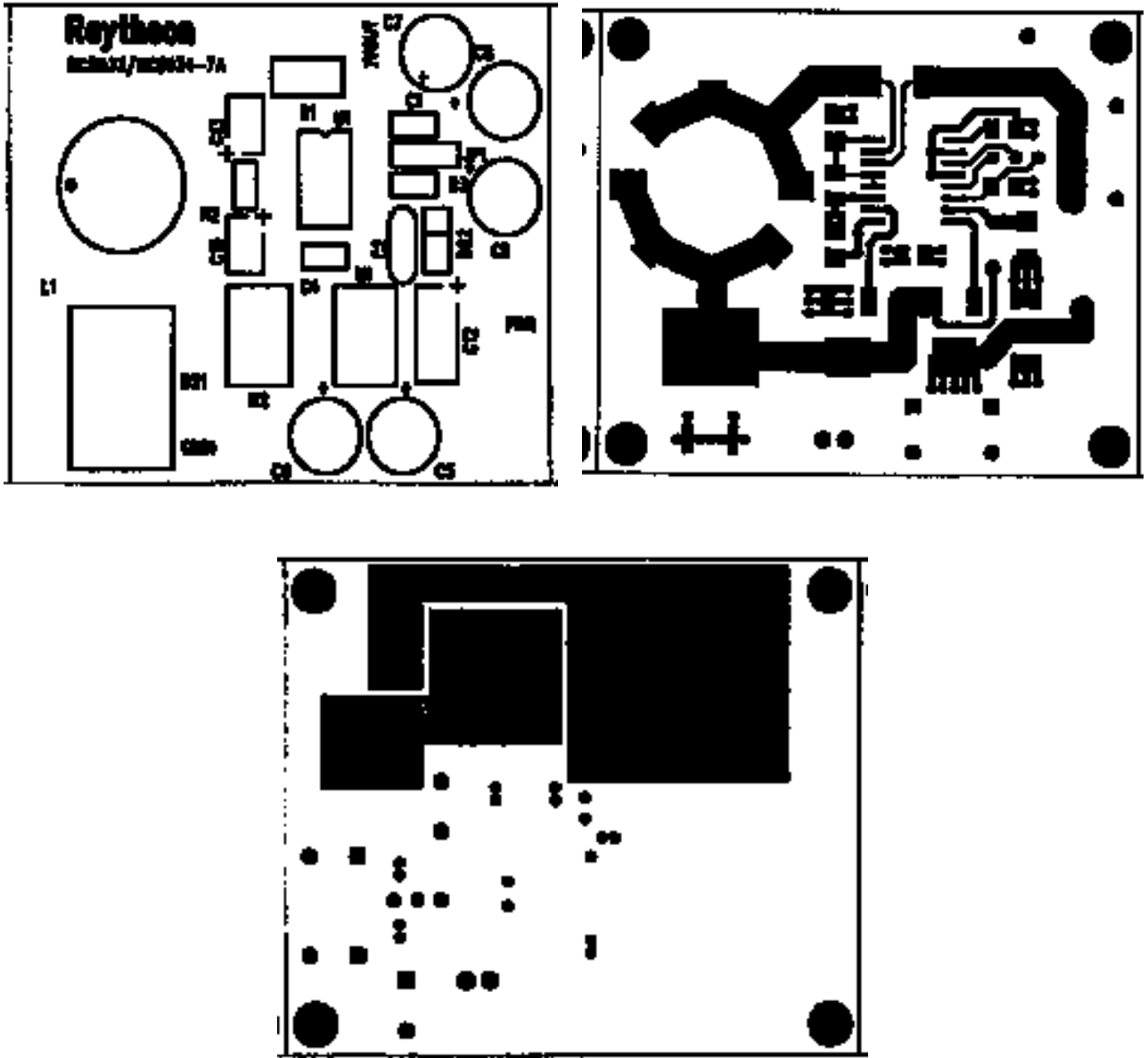


Figure 5. Sample PCB Layout

Notes:

Preliminary Information

Notes:

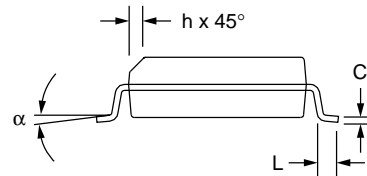
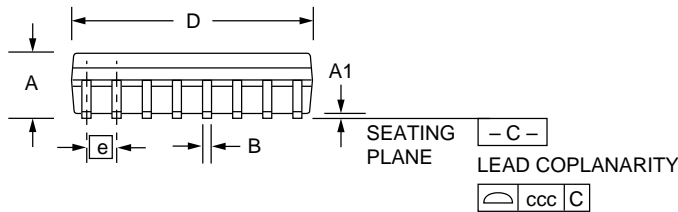
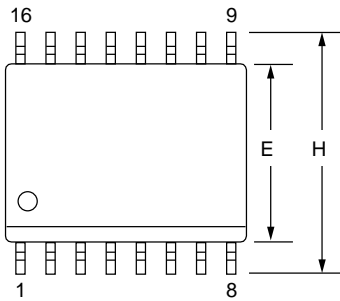
Preliminary Information

Mechanical Dimensions – 16 Lead SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Preliminary Information

Ordering Information

Product Number	Package	θ JA
RC5034M	16 SOIC	85°C/W

Preliminary Information

The information contained in this data sheet has been carefully compiled; however, it shall not by implication or otherwise become part of the terms and conditions of any subsequent sale. Raytheon's liability shall be determined solely by its standard terms and conditions of sale. No representation as to application or use or that the circuits are either licensed or free from patent infringement is intended or implied. Raytheon reserves the right to change the circuitry and any other data at any time without notice and assumes no liability for errors.

LIFE SUPPORT POLICY:

Raytheon's products are not designed for use in life support applications, wherein a failure or malfunction of the component can reasonably be expected to result in personal injury. The user of Raytheon components in life support applications assumes all risk of such use and indemnifies Raytheon Company against all damages.

Raytheon Electronics
Semiconductor Division
350 Ellis Street
Mountain View CA 94043
415 968 9211
FAX 415 966 7742